

In the Claims

1-20. Canceled

21. (New) A gain-controlled amplifier with a fixed minimum gain, comprising:

an output load (4) across which a variable gain output signal is provided;

a first gain-control output transistor (21) with its output connected to drive the output load (4) and an input to receive a first gain-control signal (16);

a second gain-control output transistor (22) with its output connected in parallel with first gain-control output transistor (21) to drive the output load (4) and an input to receive a second gain-control signal (17);

a third gain-control output transistor (23) with its output connected in shunt with the output load (4) and an input to receive said second gain-control signal (17);
and

an output-transistor signal input connected in parallel with all three of the first, second, and third gain-control output transistors (21-22);

wherein, said first and second gain-control signals (16-17) when varied relative to one another will balance the contributions of amplified output signals to the output load (4) by the first and second gain-control output transistors (21-22) and an output-load shunting effect of the third gain-control output transistor (23);

wherein, a minimum amplifier gain is determined by the combination of the output load (4) driven by the second gain-control output transistor (22) and shunted by the third gain-control output transistor (23); and

wherein, a maximum amplifier gain is determined by the combination of the output load (4) driven by the first gain-control output transistor (21).

22. The gain-controlled amplifier of claim 21, wherein:

the first, second, and third gain-control output transistors (21-23) are bipolar types and have their emitters connected in parallel, and such provides for the output-transistor signal input;

the first and second gain-control output transistors (21-22) have their collectors connected in parallel; and

the second and third gain-control output transistors (22-23) have their bases connected in parallel.

23. (New) A gain-controlled differential amplifier with a fixed minimum gain, comprising:

a differential output load (4-5) across which a variable-gain differential-output signal is provided;

a first gain-control output transistor (21) with its output connected to drive the output load (4) and an input to receive a first gain-control signal (16);

a second gain-control output transistor (22) with its output connected in parallel with first gain-control output transistor (21) to drive the output load (4) and an input to receive a second gain-control signal (17);

a third gain-control output transistor (23) with its output connected in shunt with the output load (4) and an input to receive said second gain-control signal (17);
and

a first differential output-transistor signal input connected in parallel with all three of the first, second, and third gain-control output transistors (21-22);

a fourth gain-control output transistor (31) with its output connected to drive the output load (5) and an input to receive a fourth gain-control signal (16);

a fifth gain-control output transistor (32) with its output connected in parallel with fourth gain-control output transistor (21) to drive the output load (5) and an input to receive a fifth gain-control signal (17);

a sixth gain-control output transistor (33) with its output connected in shunt with the output load (5) and an input to receive said fifth gain-control signal (17); and

a second differential output-transistor signal input connected in parallel with all three of the fourth, fifth, and sixth gain-control output transistors (31-32);

wherein, said fourth and fifth gain-control signals (16-17) when varied relative to one another will balance the contributions of amplified output signals to the

output load (5) by the fourth and fifth gain-control output transistors (31-32) and an output-load shunting effect of the sixth gain-control output transistor (33);

wherein, a minimum amplifier gain is determined by the combination of the output loads (4-5) driven by the second and fifth gain-control output transistors (22, 32) and shunted by the third and sixth gain-control output transistors (23, 33); and

wherein, a maximum amplifier gain is determined by the combination of the output loads (4-5) driven by the first and fourth gain-control output transistors (21, 31).

24. The gain-controlled differential amplifier of claim 23, wherein:

the first, second, and third gain-control output transistors (21-23) are bipolar types and have their emitters connected in parallel, and such provides for the first differential output-transistor signal input;

the fourth, fifth, and sixth gain-control output transistors (31-33) are bipolar types and have their emitters connected in parallel, and such provides for the second differential output-transistor signal input;

the first and second gain-control output transistors (21-22) have their collectors connected in parallel;

the second and third gain-control output transistors (22-23) have their bases connected in parallel.

the fourth and fifth gain-control output transistors (31-32) have their collectors connected in parallel; and

the fifth and sixth gain-control output transistors (32-33) have their bases connected in parallel.

25. (New) A gain-controlled amplifier with a fixed minimum gain, comprising:

a tapped output load (41-42) across which a variable gain output signal is provided, and including a tap (43);

a first gain-control output transistor (21) with its output connected to drive the output load (41-42) and an input to receive a first gain-control signal (16);

a second gain-control output transistor (24) with its output connected to drive said tap (43) and an input to receive a second gain-control signal (17);

an output-transistor signal input connected in parallel with all both of the first and second gain-control output transistors (21, 24);

wherein, the combination of the first gain-control output transistor (21) and the whole of the tapped output load (41-42) provide for a maximum amplifier gain;

wherein, the combination of the second gain-control output transistor (24) and the tap (43) of the tapped output load (41-42) provide for a minimum amplifier gain; and

wherein, said first and second gain-control signals (16-17) when varied relative to one another operate to balance the contributions of amplified output signals to the output load (41-42) by the first and second gain-control output transistors (21, 24).

26. The gain-controlled amplifier of claim 25, wherein:

the first and second gain-control output transistors (21, 24) are bipolar types and have their emitters connected in parallel, and such provides for the output-transistor signal input; and

the first and second gain-control output transistors (21, 24) respectively receive the first and second gain-control signals (16-17) at their bases.

27. (New) A gain-controlled differential amplifier with a fixed minimum gain, comprising:

a first tapped output load (41-42) across which a first variable-gain differential output signal is provided, and including a tap (43);

a second tapped output load (51-52) across which a second variable-gain differential output signal is provided, and including a tap (53);

a first gain-control output transistor (21) with its output connected to drive the output load (41-42) and an input to receive a first gain-control signal (16);

a second gain-control output transistor (24) with its output connected to drive said tap (43) and an input to receive a second gain-control signal (17);

a third gain-control output transistor (31) with its output connected to drive the output load (51-52) and an input to receive said first gain-control signal (16);

a fourth gain-control output transistor (34) with its output connected to drive said tap (53) and an input to receive said second gain-control signal (17);

a first output-transistor differential signal input connected in parallel with all both of the first and second gain-control output transistors (21, 24);

a second output-transistor differential signal input connected in parallel with all both of the third and fourth gain-control output transistors (31, 34);

wherein, the combination of the first gain-control output transistor (21) and the whole of the tapped output load (41-42), and the combination of the third gain-control output transistor (31) and the whole of the tapped output load (51-52), provide for a maximum amplifier gain;

wherein, the combination of the second gain-control output transistor (24) and the tap (43) of the tapped output load (41-42), and the combination of the fourth gain-control output transistor (34) and the tap (53) of the tapped output load (51-52), provide for a minimum amplifier gain; and

wherein, said first and second gain-control signals (16-17) when varied relative to one another operate to balance the contributions of amplified output signals to the output loads (41-42, and 51-52) by the first through fourth gain-control output transistors (21, 24, 31, and 34).

28. The gain-controlled differential amplifier of claim 27, wherein:

the first and second gain-control output transistors (21, 24) are bipolar types and have their emitters connected in parallel, and such provides for the first output-transistor signal input;

the third and fourth gain-control output transistors (31, 34) are bipolar types and have their emitters connected in parallel, and such provides for the second output-transistor signal input; and

the first through fourth gain-control output transistors (21, 24, 31, and 34) respectively receive the first and second gain-control signals (16-17) at their bases.